29.6 A Signal-Integrity Self-Test Concept for Debugging Nanometer CMOS ICs

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The increasing complexity of VLSI chips with nanometer feature sizes has reduced the margins in digital circuits. Voltage spikes and dips, temperature variations, cross talk, supply and substrate noise impair the power supplies. These variations depend on unforeseen operational conditions and, consequently, chips fail although they passed standard test procedures. Particularly for nanometer CMOS ICs, the large number of metal layers with the increasing metal densities (metal fill), prevents physical probing of the signals for debug purposes. To enhance observation of important design and technology parameters, such as supply noise, capacitances, temperature, threshold voltage, etc., monitors are embedded within the functional cores. Dedicated monitor circuits have been proposed [1, 2]. This paper presents a concept that deals with these problems without special requirements on technology, design, layout, testing or operation. Its constituent parts are library compliant and all communication is digital.

The signal-integrity self-test (SIST) architecture consists of three groups of elements as shown in Fig. 29.6.1. First, different design and technology monitors are placed within the functional cores of an IC. Each monitor fits into the standard-cell library design style and affects the total design as little as possible. The monitors operate at the local power supply, generate their own reference values and can be fully switched off. All analog sensing and processing as well as the conversion into a digital format is done locally. Data is transported to and from the monitors by means of a digital scan chain. This second element of the architecture provides a serial connection between the various monitors in the different cores, at minimum cost in terms of data communication and wiring. Through the scan chain a monitor is activated, its settings are controlled, and the timing window is set. The monitors have a one-bit output; the accuracy of the measurement is achieved by logarithmically stepping through the range.

The third element in this architecture is the controller. The scan-chain uses a sub-set of the IEEE1149.1 protocol and can therefore be connected to any already present scan-chain controller. The monitors allow the readout of local (within a core) signal integrity and performance parameters as well as the global distribution of these parameters. This information is used for debug and engineering purposes and for determining operating margins.

The monitors of this SIST system need to fulfill various conflicting demands. They must perform accurate measurements, although the transistor sizes are limited by the standard-cell geometry style and the wiring must accommodate the requirements of power and ground routing to the neighboring digital cells. Also the metal density rules and the different well connections of the monitors require compromises in the monitor design and layout.

Figure 29.6.2 shows the supply noise monitor. An unclocked comparator measures the voltage variations on the power supply network or power switches. With a 30GHz bandwidth, this comparator is used to detect spikes (peaks or dips) on power rails and substrate. The signals are measured via a selector that contains a fixed voltage attenuator for detecting voltage peaks exceeding the power supply. The comparison level is generated by the 7b DAC, which is controlled by the scan-chain data. Resetting the SR latch opens the measurement window; during a controlled period of time the monitored signal is checked versus the DAC value. By operating the DAC in a successive approximation way an accurate value is obtained within 7 read/write cycles. The comparator is designed for a DC-resolution of 10mV and can measure 10ps wide spikes of 20mV.

A second monitor, Fig. 29.6.3, is based on a modified temperature sensor [3]. Two diodes generate a proportional-to-absolute-temperature (PTAT) current. A resistor network and a third diode generate a temperature-independent voltage (V_{ref}=800mV), which is fed to the voltage monitor (see Fig. 29.6.2) for calibration of the voltage measurements. The scan chain delivers a four-bit value for the setting of the resistor value N_TR. Comparison of a diode voltage with a settable PTAT voltage generates temperature decisions. In the test silicon, four bits are chosen for the temperature settings, resulting in a temperature range from 0–150°C with a resolution of 10°C. More accuracy will require a larger number of bits. When active, this monitor consumes 10μA.

Figure 29.6.4 shows the library-style designed temperature monitor embedded in a digital core. This flexibility allows the monitors to be put at any location in any digital or analog core. Figure 29.6.7 shows the test chip in 90nm CMOS technology. For evaluation purposes, four identical functional cores enable different test conditions varying switching activity, power wiring resistance and decoupling capacitance. Each core of 0.7×0.7mm² consists of latches and logic, which can be programmed to a desired switching activity introducing various levels of supply noise. In order to emulate the effects of power switches and wiring, each core is connected to the power supply via four pairs of bondpads, each with a different amount of resistance. Every core contains four monitors: the two previously discussed supply noise and temperature monitors and two delay line-based technology monitors all controlled by the scan chain. The internal value of the bandgap is also available at a bond pad for characterization.

Figure 29.6.5 shows the measured behaviour of the temperature monitor: the typical bandgap curve is visible and is (untrimmed) close to the target of 800mV. Results from two lots show a standard deviation of the bandgap output voltage of 4.5mV. The step curve shows thirteen of the detected temperature ranges, measured on a digital production IC tester.

Figure 29.6.6 shows supply-voltage dip measurements with the supply-noise monitor in core B (Fig. 29.6.7), for different activity factors and at two clock frequencies. This core has only a small amount (250pF) of additional decoupling capacitance. At low activity, the clock-induced voltage dip is most important. At high activity the data-depended dips dominate.

The flexibility of the SIST concept allows the system to be easily extended with a variety of other signal-integrity and/or performance monitors.

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References:
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[2] E. Alon, et al., "Circuits and Techniques for High-Resolution Measurement of On-Chip Power Supply Noise," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 820–828, April, 2005.
[3] D. Schinkel, et al., "A 1-V 15μW High-Precision Temperature Switch," *Proc. ESSCIRC*, pp. 77 – 80, Sept., 2001.

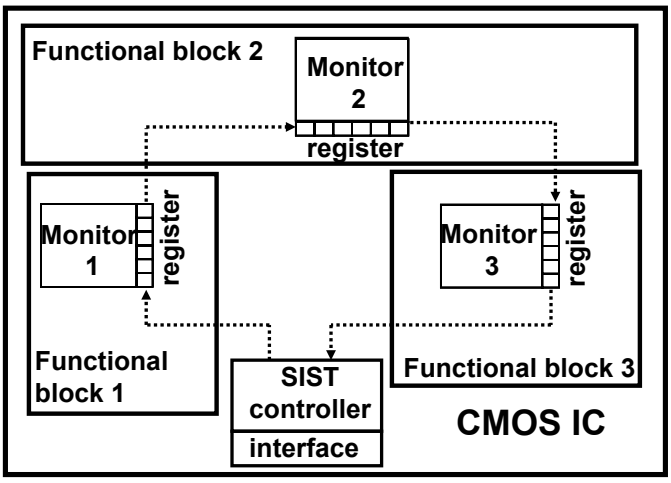

Figure 29.6.1: Architecture of the signal integrity self test system as applied in an IC layout.

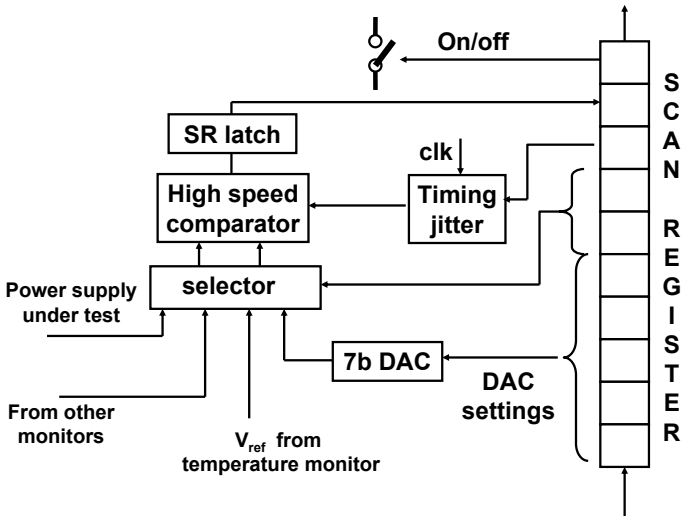

Figure 29.6.2: Block diagram of the voltage monitor.

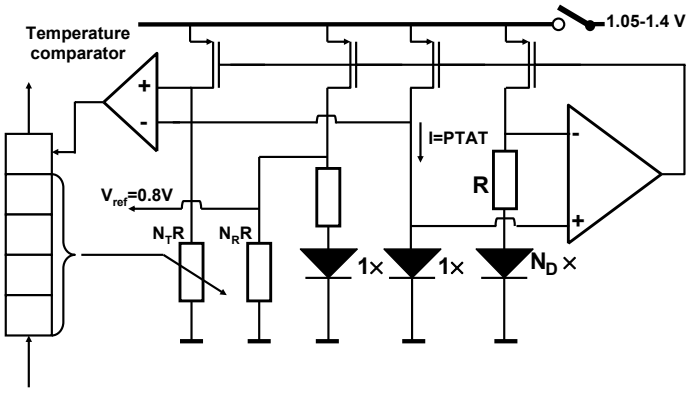

Figure 29.6.3: Detailed schematic of the temperature monitor and voltage reference.

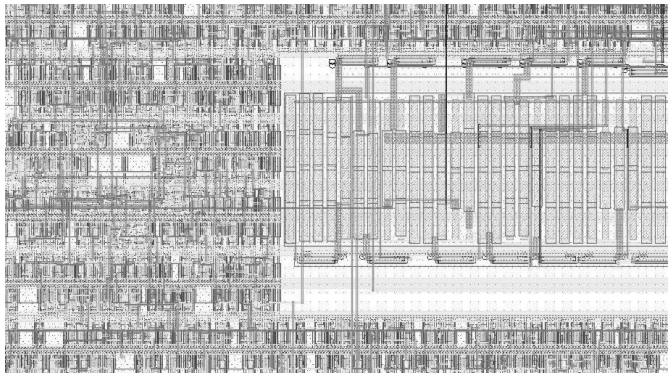

Figure 29.6.4: The layout of the resistor bank of the temperature monitor in standard-cell style (tiling patterns removed).

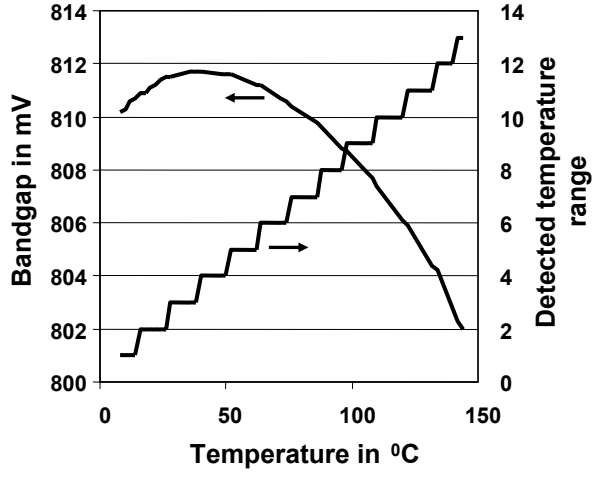

Figure 29.6.5: Measured bandgap curve and the temperature intervals as indicated by the monitor.

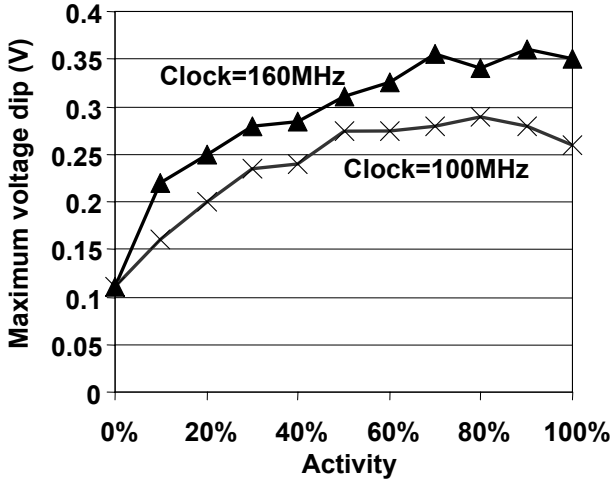

Figure 29.6.6: Measured voltage dip as a function of switching activity for 100 and 160MHz clock frequency.

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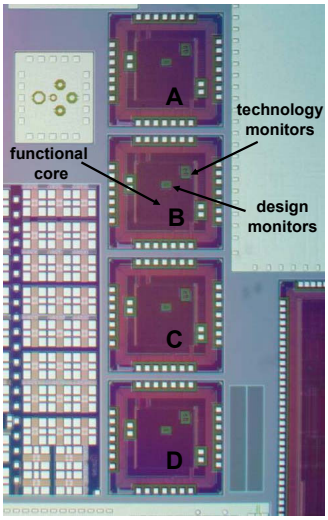

Figure 29.6.7: Die micrograph of four functional cores, each with embedded SIST monitors.

